AMENDMENTS TO THE DRAWINGS

The attached drawing sheet includes changes to Fig. 12, which are that of . This sheet replaces the original sheet including Fig. 12.

Attachments: Replacement Drawing Sheet

REMARKS

Claims 7 and 8 are pending in this application. Claim 7 has been amended. No new matter has been added.

Claim Rejections under 35 U.S.C. §103

Claims 7 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Prior Art, Figure 12 in view of Yamaguchi et al., Japan Publication No. 62-37463. Applicants request reconsideration of the rejection for the following reasons.

Claim 7 has been amended by adding the limitation that the source voltage detector and light-emission cutoff circuit comprise transistors of bipolar type. Support in the specification and drawings for the added limitation is provided by the second embodiment of the invention, for example, shown in Figure 5. Applicants further note the description on page 13, lines 18-21 of the specification, which sets forth that the transistors used in the circuit configuration of Figure 5 are of bipolar type, thereby facilitating integration of the optical transmitter into one chip.

As set forth in the Office Action, the prior art shown in Figure 12 of the present application differs from claim 7 in that the prior art does not disclose a circuit for comparing whether the detected source voltage is lower than a predetermined voltage and cutting off the supply of the drive current to the light-emitting element when the monitored source voltage is lower than the predetermined voltage. Yamaguchi is relied upon for disclosing this deficiency.

In particular, Yamaguchi is relied upon for disclosing a data link driving circuit having voltage detecting means 9 for comparing a source voltage with a reference threshold voltage, and if the detected source voltage is lower than the predetermined voltage, it will cut off the supply of the drive current to the light-emitting element. However, Yamaguchi does not disclose the circuit of the invention set forth in claims 7 and 8, as amended, wherein the source voltage detector and light-emitting cutoff circuit are comprised of transistors of bipolar type.

In Yamaguchi, the voltage detecting means 9 is a CMOS LSI circuit, which differs from that of a circuit having transistors of the bipolar type. The source voltage detector having bipolar transistors of the claimed invention operates at a higher speed than that of the comparable CMOS circuit of Yamaguchi, which is an advantage not

appreciated by the admitted prior art or the reference. Accordingly, the combination of the prior art of Figure 12 and Yamaguchi does not render the claimed invention obvious under 35 U.S.C. §103 and the rejection should be withdrawn.

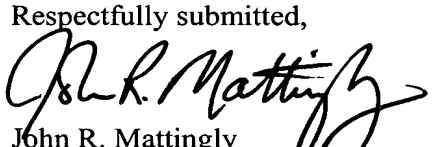
Drawings

Figure 12 has been labeled "PRIOR ART" as suggested by the Examiner on page 2 of the Office Action.

CONCLUSION

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



John R. Mattingly
Registration No. 30,293
Attorney for Applicant(s)

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 Diagonal Road, Suite 370
Alexandria, Virginia 22314
(703) 684-1120
Date: October 12, 2005